IN THE CLAIMS

Please cancel claims 1-12 without prejudice.

Please amend claims 15 and 16 as follows below.

Please add new claims 17-34 that follow below.

Please accept a clean version of the entire set of pending claims as amended by this response.

CLEAN CLAIMS ARE AS FOLLOWS

1-12. (Cancelled)

13. (Unamended) A method for assembling an electronic package, comprising:

forming a housing which has a bond pad located on a bond shelf which has an edge;

forming a conductive strip along the edge of the bond shelf;

removing a portion of the conductive strip.

14. (Unamended) The method as recited in claim 13, wherein

the conductive strip is formed by plating a conductive material onto the edge.

15. (Amended Once) The method as recited in claim 13, wherein

the portion of the conductive strip is removed by drilling a portion of the bond shelf.

16. (Amended Once) The method as recited in claim 13, further comprising:

mounting an integrated circuit to the housing and connecting the integrated circuit to the bond pad.

17. (New) The method as recited in claim 13, wherein the portion of the conductive strip is removed by etching away a portion of a conductive material on the bond shelf.

18. (New) The method as recited in claim 13, wherein the conductive strip is formed along the edge of the bond shelf by

masking all surfaces except for the edge of the bond shelf, and

plating a conductive material onto the edge of the bond shelf.

19. (New) The method as recited in claim 18, wherein the conductive material is copper, and the conductive strip is further formed by plating gold onto the copper.

20. (New) The method as recited in claim 19, wherein the portion of the conductive strip is removed by drilling a portion of the bond shelf.

21. (New) A method of forming an integrated circuit package, comprising:

providing a package housing having a first plurality of bonding pads located on a first bond shelf, the first bond shelf having a first edge;

forming a first conductive strip along the first edge of the first bond shelf, the first conductive strip wrapping around the edge of the first bond shelf from at least one of the first plurality of bonding pads on the first bond shelf to a first conductor under the first bond shelf; and,

removing a portion of the first conductive strip.

22. (New) The method as recited in claim 21, wherein

the first conductive strip is formed by plating a conductive material onto the first edge.

23. (New) The method as recited in claim 21, wherein the first conductor under the first bond shelf is a power bus.

24. (New) The method as recited in claim 21, wherein the first conductor under the first bond shelf is a routing trace.

25. (New) The method as recited in claim 21, wherein the portion of the first conductive strip is removed by drilling a portion of the first bond shelf.

26. (New) The method as recited in claim 25, wherein the portion drilled in the first bond shelf is a notch.

27. (New) The method as recited in claim 21, wherein the portion of the first conductive strip is removed by etching away a portion of the first conductive strip of the first bond shelf.

28. (New) The method as recited in claim 21, wherein the package housing is provided by

forming a first conductive layer on a first dielectric substrate,

placing a second dielectric substrate on the first conductive layer of the first dielectric substrate, the second dielectric substrate having a second conductive layer, and

etching the second conductive layer to form the first plurality of bonding pads.

29. (New) The method as recited in claim 28, wherein the first conductive layer forms the first conductor under the first bond shelf.

30. (New) The method as recited in claim 28, wherein the etching of the second conductive layer to further form a second conductor, and

the package housing has a second plurality of bonding pads located on a second bond shelf, the second bond shelf having a second edge, the package housing is further provided by

placing a third dielectric substrate on the

second conductive layer of the second dielectric substrate, the third dielectric substrate having a third conductive layer, and

etching the third conductive layer to form a second plurality of bonding pads,

and

the method further includes

forming a second conductive strip along the second edge of the second bond shelf, the second conductive strip wrapping around the second edge of the second bond shelf from at least one of the second plurality of bonding pads on the second bond shelf to the second conductor under the second bond shelf.

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31. (New) The method as recited in claim 30, wherein the second conductive layer forms the second conductor under the second bond shelf.

32. (New) The method as recited in claim 30, wherein the second conductive strip is formed by plating a conductive material onto the second edge.

33. (New) The method as recited in claim 30, wherein the second conductor under the second bond shelf is

a power bus.

34. (New) The method as recited in claim 30, wherein the second conductor under the second bond shelf is a routing trace.